a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween, where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is a multiple of m;

said memory control means including counter means, responsive to receipt on said processor data bus of [a row] an address including a row address and a part of a column address specified by said processor means to specify an n-bit data word in said memory means, for successively generating [n] n/m column addresses, applying the received row address and [m of] the generated column addresses on said memory data bus to transfer data between said memory means and said data processor means, with the data transfer including transfer of m bits of data in parallel between said memory means and said memory control means, and transfer of n bits of data between said memory control means and said data processor means.

11. (amended) A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing pixel information;

data processing means for specifying addresses of memory location in said memory means for retrieval of pixel